ABSTRACT

Packet buffer equipment in which a buffer and time for packet assembly is utilized for packet header analysis and addition processing to obtain increased efficiency. The equipment aims to receive virtual channel (VC)-multiplexed ATM cells to assemble into a packet on a VC basis maintaining each received cell, to output on a packet basis. As an embodiment, cells are assembled into a packet by storing cells from the top cell to the end cell into a packet buffer memory consisting of a plurality of cell buffers to store cells. Also, a sequence controller is provided for detecting the write completion of a new header cell, and for connecting a packet in packet-under-assembly queue constituted by under-assembly pointer into an output-wait queue.